APPLICATION NOTE

The content of this note is based on information received from manufacturers in the electrical and electronics industries or their representatives and does not imply practical experience by Elektor Electronics or its consultants.

digitally-controlled potentiometers

with integrated voltage comparators

Although microprocessors are integrated into more and more electronic circuits, there remain requirements for analogue components and devices. One such is the potentiometer, which, until now, has been difficult to emulate by a digital equivalent. Xicor have overcome this difficulty with their X9440 and X9448. These devices combine the flexibility of an analogue product with the power of digital communications.

A Xicor Application

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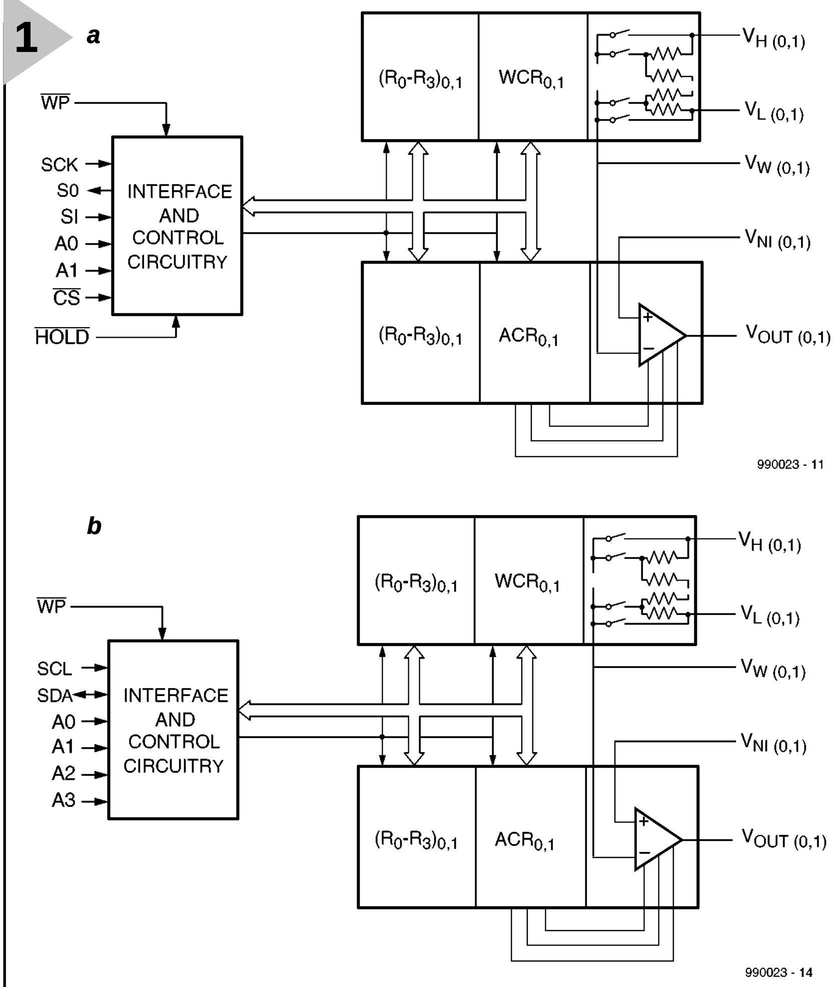

Figure 1. Functional diagram of the X9440 (a) and the X9448 (b). Differences between the two concern mainly the serial interface.

DESCRIPTION

Xicor's X9440 and X9448 integrate two non-volatile (EEPOT) digitally-controlled potentiometers and two voltage comparators on a CMOS monolithic microcircuit.

Both types contain two resistor arrays, each composed of 63 resistive elements. Between successive elements and at either end are tap points accessible to the wiper elements. The position of the wiper element on the array is controlled by the user through the serial bus interface.

Each potentiometer has an associated voltage comparator, which compares the external input voltage, V_{NI}, 2

REGISTER BIT DESCRIPTIONS

Wiper Counter Register (WCR)

0	0	WP5	WP4	WP3	WP2	WP1	WP0
		(volatile)					(LSB)

WP0-WP5 identify wiper position.

Analog Control Register (ACR)

0	0	User-bit5	User-bit4	User-bit3	Latch	Enable	Shut-down
			(volatile)				(LSB)

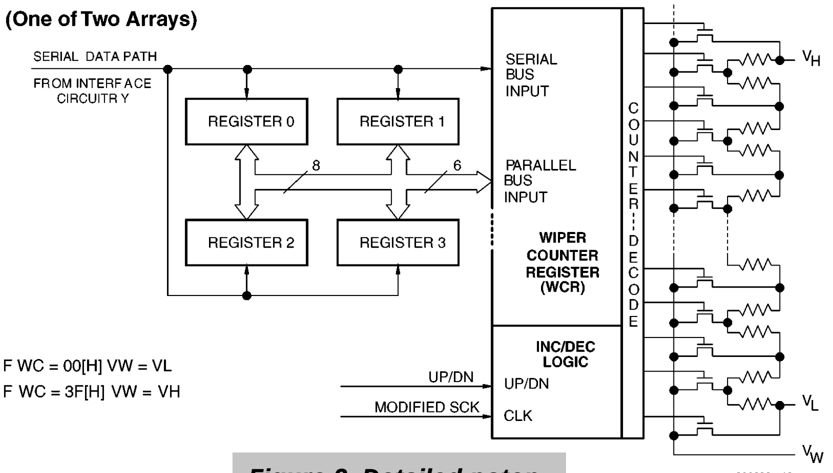

Figure 2. Detailed potentiometer block diagram.

with the wiper voltage, V_W, and sets the output voltage level to a logic high or low.

Each resistor array and comparator has associated with it a wiper counter register (WCR), analogue control register (ACR), and eight 6-bit data registers that can be directly written and read by the user.

The contents of the wiper counter register control the position of the wiper on the resistor array.

The contents of the analogue control register control the comparator and its output.

The potentiometer is programmed via a serial interface (X9440: SPI; X9448: two-wire).

ARRAY DESCRIPTION

The integrated circuits comprise two resistor arrays and two voltage comparators. Each array contains 63 resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H and V_L inputs).

At both ends of each array and between successive resistive segments is a CMOS switch connected to the wiper (V_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by a volatile wiper counter register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and WCR can be read and written by the host system.

SERIAL INTERFACE

The X9440 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ pins must be HIGH during the entire operation.

The SO and SI pins can be connected together since they have three-state outputs. This may help to reduce system pin count.

The X9448 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data on to the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9448 will be considered a slave device in all applications.

Clock and data conventions (X9448)

Data states on the SDA line can change only during SCL LOW periods (t_{LOW}). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

Start condition (X9448)

All commands to the X9448 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH (t_{HIGH}). The X9448 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

Stop condition (X9448)

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

Acknowledge (X9448)

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9448 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte, the X9448 will respond with a final acknowledge.

VOLTAGE COMPARATOR

The comparator compares the wiper voltage, V_W, with the external input voltage, V_{NI}. The comparator and its logic level output are controlled by the Shutdown, Latch, and Enable bits of the Analogue Control Register (ACR).

Enable connects the comparator output to the V_{OUT} pin, Latch memorizes the output logic state, and Shutdown removes the analogue section supply voltage to save power. The ACR is programmed via the SPI (X9448: two-wire) serial interface.

The ACR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the ACR. These data registers and the ACR may be read and written by the host system.

WCR AND ACR

The X9440 contains two Wiper Counter Registers, WCR, one for each EEPOT potentiometer, and two Analogue Control Registers, ACR, one for each of the voltage comparators. The WCR is equivalent to a serial-in, parallel-out counter with its outputs decoded to select one of sixty-four switches along its resistor array.

The contents of the WCR and ACR can be altered in four ways: they may be written by the host via the Write WCR instruction (serial load); they may be written indirectly by transferring the contents of one of four associated data registers (DRS) via the XFR Data Register instruction (parallel load); they can be modified one step at a time by the Increment/Decrement instruction (WCR only). Finally, they may be loaded with the contents of their data register zero (R0) upon power-up.

The WCR and ACR are volatile registers; that is, their contents are lost when the X9440 is powered-down.

Although the registers are automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

Programming the ACR is similar to the WCR. However, the six bits in the WCR position the wiper in the resistor array, whereas three bits in the ACR control the comparator and its output.

DATA REGISTERS

Each potentiometer and each voltage comparator has four non-volatile Data Registers (DR). These may be read or written directly by the host and data can be transferred between any of the four DRS and the WCR or ACR. It should be noted that all operations changing data in one of these registers are non-volatile and will take not more than 10 ms.

If the application does not require storage of multiple settings for the potentiometer or comparator, the registers may be used as regular memory locations for storing system parameters or user preference data.

Detailed datasheets for the X9440 and X9448 may be found on the Internet: **http: //www.xicor.com**

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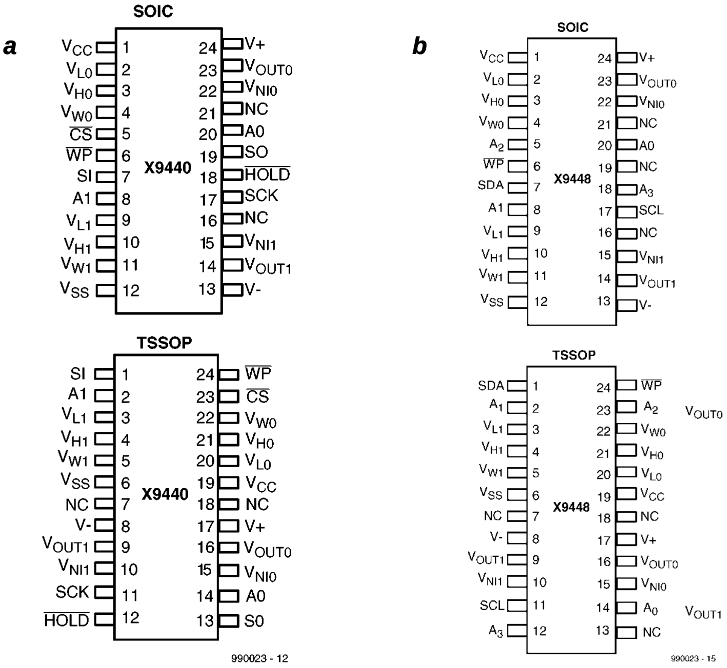

Figure 3. Pin configuration of the X9440 (a) and the X9448 (b). Both devices are available in 24-lead TSSOP and 24-lead SOIC packages.

PIN DESCRIPTIONS

Host interface pins (X9440)

Serial output (SO)
SO is a push/pull serial data output pin. During a read cycle, data is shifted out via this pin. Data is clocked out by the trailing edge of the serial clock.

Serial input (SI)
SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input via this pin. Data is latched by the leading edge of the serial clock.

Serial clock (SCK)
The SCK input is used to clock data into and out of the X9440/X9448.

Chip select ($\overline{\text{CS}}$)
When $\overline{\text{CS}}$ is HIGH, the X9440 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. $\overline{\text{CS}}$ LOW enables the X9440, placing it in the active power mode.

Hold ($\overline{\text{HOLD}}$)
$\overline{\text{HOLD}}$ is used in conjunction with the $\overline{\text{CS}}$ pin to select the X9440. Once it is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{\text{HOLD}}$ must be made LOW while SCK is LOW. To resume communication, $\overline{\text{HOLD}}$ is made HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{\text{HOLD}}$ should be held HIGH at all times.

Device address (A_0–A_1)
The address inputs are used to set the least significant two bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9440. A maximum of four devices may share the same SPI serial bus.

Host interface pins (X9448)

Serial clock (SCL)
The SCL input is used to clock data into and out of the X9448.

Serial data (SDA)
SDA is a bidirectional pin used to transfer data into and out of the X9448.

Device address (A_0–A_1)
The address inputs are used to set the least significant four bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9448. A maximum of 16 devices may share the same 2-wire serial bus.

Potentiometer pins

V_H (V_{H0}–V_{H3}), V_L (V_{L0}–V_{L3}) (X9440)
V_H (V_{H0}–V_{H1}), V_L (V_{L0}–V_{L1}) (X9448)
The V_H and V_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_W (V_{W0}–V_{W1})
The wiper output, V_W, is equivalent to the wiper output of a mechanical potentiometer and is connected to the inverting input of the voltage comparator.

Comparator and device pins

Voltage input V_{NI0}, V_{NI1}
V_{NI0} and V_{NI1} are the input voltages to the plus (non-inverting) inputs of the two comparators.

Buffered voltage outputs, V_{OUT0}, V_{OUT1}
V_{OUT0} and V_{OUT1} are the buffered voltage comparator outputs controlled by bits in the volatile ACR.

Hardware write protect input, $\overline{\text{WP}}$
The $\overline{\text{WP}}$ pin when low prevents non-volatile writes to the WCR and ACR.

Analogue supplies, V+, V–
The analogue supplies, V+ and V– are the supply voltages for the EEPOT analogue section and the voltage comparators.

System supply V_{CC} and ground V_{SS}
The system supply, V_{CC}, and its reference, V_{SS}, are used to bias the interface and control circuits.